REMARKS

Claims 1 - 8 stand rejected "under 35 U.S.C. §103 as being unpatentable over the admitted prior art." Applicant respectfully traverses these rejections for the following reasons.

35 U.S.C. §103 recites in part:

> [a] patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

Hence, 35 U.S.C. §103 authorizes a rejection where to meet the claim, it is necessary to modify a single reference or to combine it with one or more other references. To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. See, M.P.E.P. 706.02(j).

The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and

not based on applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

The Examiner argues Applicant's invention differs from the "admitted prior art" by expanding the number of channels of member 17, and that doing such would have been obvious to one of ordinary skill in the art.

Applicant respectfully points out the present invention, as embodied within the current claims, is not for increasing the number of channels, but for simplifying the testing of a complex system comprised of several printed circuit boards or subsets through adaptively learning the systems topology. See, specification, page 4, lines 9-16.

Claim 1 recites "[a] testable electronic system including testable elements . . . the system including master switches (24) which define respective sub-sets (20) of elements, a specific channel of each master switch being reserved to access an identifier (22) characterizing the test organization of the associated sub-set."

The "prior art" Examiner references, I.E.E.E. standard 1149.1-1990, entitled I.E.E.E. Standard Test Access Port and Boundary-scan architecture, defines a test interface, with identifiers, for components, integrated circuits for example. In contrast, Claim 1 of the present application includes defining identifiers for sub-sets, or groups of

components, printed circuit boards for example.

This improvement is significant, at least by virtue of its ability to simplify, or in some circumstances even eliminate, the intensive task of updating a system database in cases of system evolution.

Applicant therefore respectfully submits the I.E.E.E. standard does not disclose, teach or suggest the use of identifiers for subsets of components as claimed by Applicant, but only for components individually. And, additionally requests the Examiner, if persistent in the contention Applicant's present claims are obvious in light of this prior art, particularly identify those portions of the relevant prior art where such disclosures or suggestions can be found.

The Examiner has also conceded the present invention differs due to the inclusion of stacking member 17, but argues that such inclusion is of a common technique to increase capacity, and has cited the Powers et al. reference (USP 5,651,110) in support of this contention. Applicant respectfully deems this argument moot in view of the foregoing discussion. Nevertheless, Powers teaches "a method and apparatus for controlling data flow between a computer and a plurality of memory devices which can handle component failure in a manner transparent to the computer." Column 1, lines 52-56.

Applicant respectfully submits the vertical-stacking, as referred to

by the Examiner, taught within Powers is for facilitating a backup system, which is transparent to the computer, in case of a controller failure. It has nothing to do with Applicant's invention for simplifying the testing of a complex system comprised of several printed circuit boards or subsets through adaptively learning a systems topology. Thus, it is not unexpected that it fails to disclose, teach or suggest the use of identifiers for subsets of components as claimed by Applicant.

In Powers, the first level controllers are for routing data to the second level controllers. See, column 1, lines 63-65. In case of a second level controller failure, the first level controller associated therewith will route data to other, proper functioning, second level controllers. See, column 2, lines 11-20.

Therefore, Applicant respectfully submits because both the I.E.E.E. standard and Powers fail to disclose the use of identifiers for subsets of components as claimed by Applicant individually, the combination thereof likewise fails to disclose, teach or suggest the same. Accordingly, Applicant respectfully submits his invention as embodied within the current claims would not have been obvious to a person having ordinary skill in the art to which this subject matter pertains at the time of invention.

Alternatively, Applicant submits due to the unlike nature of the Powers subject matter compared to that of the I.E.E.E. standard, no

motivation or suggestion exists, either in the references themselves, or in the knowledge generally available to one of ordinary skill in the art, at the time of invention, to combine these references. If the Examiner believes such motivation is apparent, Applicant respectfully requests the Examiner cite those portions of those references which particularly suggest this.

Supplementarily, Applicant acknowledges the Examiner's observance of one of the improvements embodied within Claim 1 of the current application, namely the use of a specific channel to reduce testing time. Applicant is unsure of the significance of the Examiner's comments with regard thereto. If the Examiner intends to base a 35 U.S.C. §103 rejection thereon, Applicant respectfully requests the Examiner clarify, and cite a reference in support of his position, as Applicant believes Claim 1, which includes the recitation of "a specific channel of each master switch being reserved to access the identifier" patentably distinguishes over the cited references

Wherefore, Applicant respectfully traverses and respectfully requests removal of the 35 U.S.C. §103 rejection to Claim 1 of the current application.

Applicant respectfully submits Claims 2 - 8 are similarly distinguishable, at least by virtue of their dependency from a patentable base claim. Wherefore, Applicant analogously traverses and respectfully

requests removal of the 35 U.S.C. §103 rejections to Claims 2 - 8 of the current application also.

CONCLUSION

In final summation, Applicant submits Claims 1 - 8 are in condition for allowance, early notification of which is earnestly solicited. Should there be any questions or other matters whose resolution may be advanced by a telephone call, the Examiner is cordially invited to contact Applicant's undersigned attorney at his number listed below.

FEES

If there are any fees due and owing in respect to this amendment, the Examiner is authorized to charge such fees to deposit account number 16-2131.

Respectfully submitted,

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